CLAIMS

What is claimed is:

1. A micro-system for burn-in system program from a plug-able subsystem into a main memory, comprising:

a processor for sending out a first control signal and a second control signal;

a main memory connected electrically with said processor for transferring data between said processor and said main memory;

a device for adjusting to first level connected electrically with said processor for receiving said first control signal and connected electrically with said main memory for changing the level of a third control signal to a first level to enable said main memory; and

a plug-able subsystem with a backup memory connected electrically with said processor for receiving said second control signal, wherein the data are transferred between said backup memory and said processor when said second control signal is at said first level, and said plug-able subsystem sends out a forth control signal to said main memory for changing said third control signal to a second level to disable said main memory, the data are not transferred between said backup memory and said processor when said second control signal is at said second level, and said third control signal is at said first level to enable said main memory for transferring data between said processor and said main memory.

2. The micro-system according to claim 1, wherein said second level is higher than said first level.

3. The micro-system according to claim 1, wherein said device for adjusting to first level includes a first grounded resistor.

4. The micro-system according to claim 1, wherein transferring data between said processor and said main memory includes the steps of:

establishing a first bus for transferring the address codes and a second bus for transferring the data codes between said processor and said main memory; and

transferring the data codes mapped to the address codes to the processor via said second bus after said main memory receiving a first read signal.

5. The micro-system according to claim 4, wherein transferring data between said processor and said main memory further comprises the step of:

writing the data codes mapped to the address codes to said main memory via said second bus after said main memory receiving a first write signal.

6. The micro-system according to claim 1, wherein transferring data between said processor and said backup memory includes the steps of:

establishing said first bus for transferring the address codes and said second bus for transferring the data codes between said processor and said backup memory; and

transferring the data codes mapped to the address codes to the processor via said second bus after said backup memory receiving a second read signal.

7. The micro-system according to claim 6, wherein said plug-able subsystem comprises:

a connector connected electrically with said processor and said main memory; and

a device for adjusting to second level connected electrically with said connector for sending out said forth control signal through said connector to change the level of said third control signal.

8. The micro-system according to claim 7, wherein said device for adjusting to second level includes a second resistor connected to a power.

9. The micro-system according to claim 7, wherein said connector is a slot.

10. The micro-system according to claim 1, wherein said main memory is a non-volatile memory.

11. A method for burn-in the system program from a plug-able subsystem into a main memory in a micro-system, wherein said micro-system includes a processor, said main memory, a device for adjusting to first level to enable said main memory, and said plug-able subsystem with a backup memory, comprising the steps of:

sending out a first control signal for changing the level of a third control signal and a second control signal to said plug-able subsystem from said processor, wherein the level of said second control signal level is at a first level to enable said plug-able subsystem, and the level of said third control signal is changed to said first level by said device for adjusting to first level;

sending out a forth control signal from said plug-able subsystem for changing the level of said third control signal to a second level to disable the main memory;

transferring data between said backup memory and said processor;

sending out said second control signal to said plug-able subsystem from said processor, wherein said second control signal is at said second level to disable the plug-able subsystem and said forth control signal is not sent out from said plug-able subsystem again; and

transferring data between said main memory and said processor.

12. The method according to claim 11, wherein said second level is higher than said first level.

13. The method according to claim 11, wherein said device for adjusting to first level includes a first grounded resistor.

14. The method according to claim 11, wherein transferring data between said processor and said backup memory includes the steps of:

establishing a first bus for transferring the address codes and a second bus for transferring the data codes between said processor and said backup memory; and

transferring the data codes mapped to the address codes to the processor via said second bus after said backup memory receiving a second read signal.

15. The method according to claim 11, wherein transferring data between said processor and said main memory includes the steps of:

establishing said first bus for transferring the address codes and said second bus for transferring the data codes between said

processor and said main memory; and

transferring the data codes mapped to the address codes to the processor via said second bus after said main memory receiving a first read signal.

16. The method according to claim 15, wherein transferring data between said processor and said main memory further comprises the step of:

writing the data codes mapped to the address codes to said main memory via said second bus after said main memory receiving a first write signal.

17. The method according to claim 14, wherein said plug-able subsystem further comprises:

a connector connected electrically with said processor and said main memory; and

a device for adjusting to second level connected electrically with said connector for sending out said forth control signal through said connector to change the level of said third control signal.

18. The method according to claim 17, wherein said device for adjusting to second level has a second resistor connected to a power.

19. The method according to claim 17, wherein said connector

is a slot.

20. The method according to claim 11, wherein said main memory is a non-volatile memory.